MG2470B

Thermal Resistance

V1.0

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Appendix B

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Revision History

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1 Introduction

Thermal resistance of a semiconductor package is the measure of the package's ability to transfer the heat from IC chip (wafer-die) to the ambient or PCB board. Thermal resistance is calculated by the difference between Tj (Junction Temperature) and Ta (Ambient Temperature), under the condition that the IC package dissipates electric power of 1W.

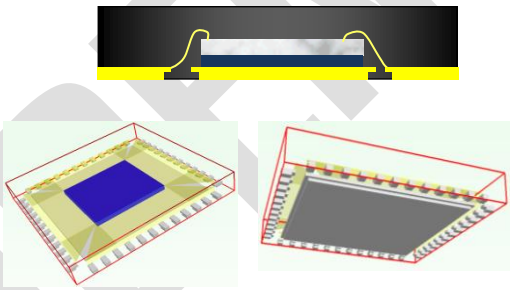
In this appendix, the simulation model and conditions for MG2470B package are described, and the result of the simulation, thermal resistances and the maximum junction temperature calculated from chip power dissipation are shown. This thermal resistance simulation had been done by HanaMicron.

2 Simulation Model and Conditions

2.1 Simulation Model

The simulation model for thermal resistance of MG2470B package is summarized in table 1. The model includes package dimensions such as mold cap thickness, wire diameter, lead frame width, lead frame thickness, lead frame pitch and overall package height. And, it also considers die physicals such as die thickness and die size.

Table 1 Simulation Model

		MG2470 (7X7 / 48LD)
Image		
PKG	Mold cap thickness	0.50mm
	Die thickness	0.17mm
	Die size	***3.09 X 3.21mm***
	Gold wire	0.80mil
	Lead frame count	***48ea***
	Lead frame Width	0.2mm
	Lead frame thickness	0.15mm
	Lead frame pitch	***0.5mm***
Overall PKG height		0.85mm

2.2 Conditions

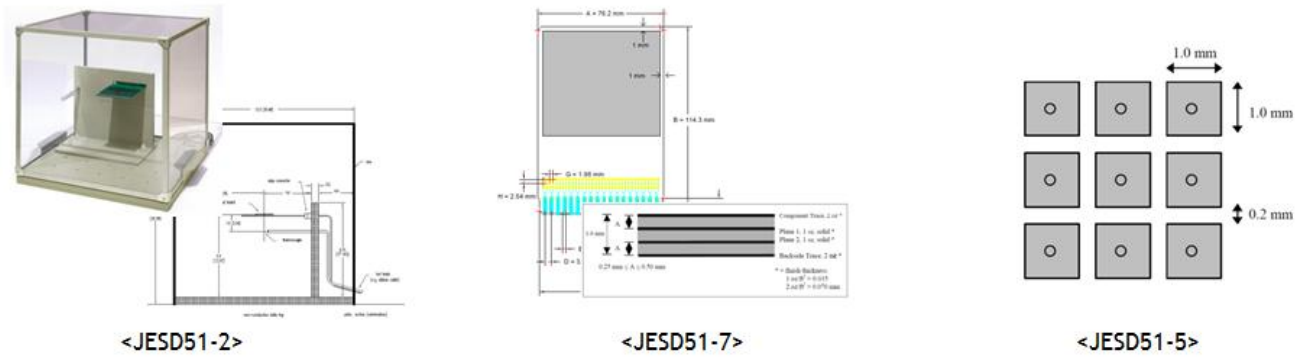
The simulation conditions include material properties, thermal test standards, and boundary conditions. Table 2 summarized material properties for mold, die, attach adhesive, wire, and lead frame. The thermal test followed the thermal test standards in Fig. 2. JESD51-2 is Environmental standard, JESD51-7 and JESD51-5 is standard for test board and thermal via respectively.

The boundary conditions for the simulation are as follows.

- Ambient temperature: 85
- Flow: Natural convection (laminar flow)
- Power: 0.07W

Table 2 Material Properties

Items	Density(kg/m^3)	Specific Heat(J/kg-K)	Thermal Conductivity(w/m-k)
Mold	1120.0	750.00	1.00
Die	2330.00	339.16	180.00
Attach Adhesive	2800.00	1400.00	3.10
Wire	19320.00	215.00	301.00
Lead frame	8940.70	215.00	46.00



<JESD51-2> <JESD51-7> <JESD51-5>

Figure 1 Thermal test standards

3 Simulation Results

Simulation results are summarized in table 3. The thermal resistance of 1S PCB is almost twice that of 2S2P PCB. Maximum thermal resistance is 95℃ for 2S2P PCB and 100℃ for 1S PCB, considering power dissipation of 0.21 mW (which is 3 times that of real chip) and margin.

Table 3 Simulation Results

	MG2470 (Die-3.09 X 3.21mm / Lead-48ea)	
	JEDEC 2S2P (4 Layer)	JEDEC 1S (1 Layer)
Thermal Resistance (Junction to Ambient) (℃/W)	25.109	49.594
Thermal Resistance (Junction to Case) (℃/W)	0.289	0.566
Maximum Junction Temperature(℃)	95	100

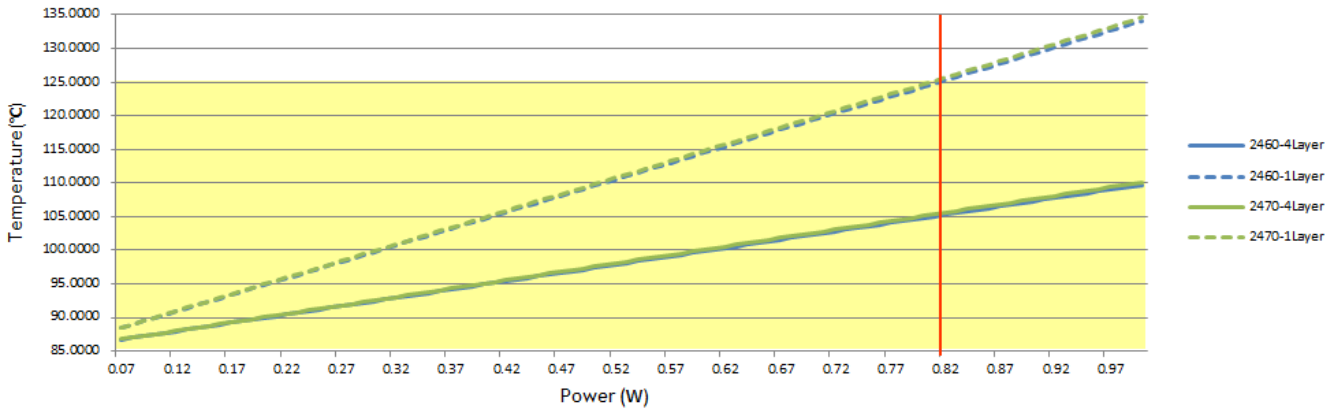


Figure 2 Junction temperature vs. the power dissipation in chip

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